# PATENT ABSTRACTS OF JAPAN

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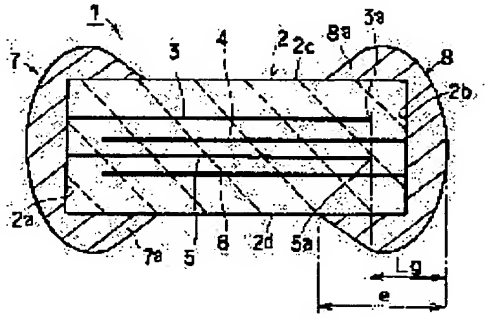
## (54) MULTILAYER CERAMIC ELECTRONIC COMPONENT

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a multiplayer ceramic electronic component with good reliability in which the cracking of sintered ceramic is hardy developed even when subjected to heat shock or stress caused by flexure of a printed circuit board after the component is mounted thereon.
SOLUTION: Inner electrodes 3-6 are provided in a sintered ceramic 2 and first and second outer electrodes 7, 8 are formed to cover the first and second end faces 2a, 2b wherein the first and second outer electrodes 7, 8 have electrode covering parts 7a, 8a extending to the upper and lower surfaces 2c, 2d and the opposite side faces of the sintered ceramic. A relation $1.5\times Lg\leq e\leq 3.5\times Lg$ is satisfied, where e is the distance between the outermost side end of the outer electrodes 7, 8 and the innermost side end of the electrode covering parts 7a, 8a of the outer electrodes 7, 8, and Lg is the distance between the outermost side end of the outer electrodes 7, 8 and the forward end of the inner electrode connected electrically with the outer electrodes 7, 8 on the opposite side.

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* NOTICES *



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CLAIMS

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[Claim(s)]
[Claim 1] Two or more internal electrodes which are arranged so that it may overlap in the thickness direction through a ceramic layer in the ceramic sintered compact which has the 1st and 2nd end face which counters each other, and said ceramic sintered compact, and were pulled out by the 1st or 2nd end face, It has the 1st and 2nd external electrode formed so that the 1st and 2nd end face which said ceramic sintered compact counters for each other might be covered, respectively. It has ****-ed [ electrode ] to which the said 1st and 2nd external electrode reaches not only the 1st or 2nd end face of a ceramic sintered compact but a top face, an inferior surface of tongue, and a both-sides side. The outermost side edge of an external electrode, When distance between the inside edges of ****-ed [ electrode ] of this external electrode is set to e and distance between the outermost side edge of this external electrode and the tip of the internal electrode electrically connected to the external electrode of the opposite side is set to Lg Laminating ceramic electronic parts characterized by being constituted so that 1.5xLg<=e<=3.5xLg may be filled.
[Claim 2] Laminating ceramic electronic parts according to claim 1 with which distance e and distance Lg are constituted so that 2.0xLg<=e<=3.5xLg may be filled.
[Claim 3] Laminating ceramic electronic parts according to claim 1 or 2 which said ceramic sintered compact is constituted using the dielectric ceramics, and are used as the multilayer capacitor by it.

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## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the laminating ceramic electronic parts with which electrode structure was improved by the detail more about laminating ceramic electronic parts, such as a multilayer capacitor and a laminating varistor.
[0002]
[Description of the Prior Art] Drawing 3 is drawing of longitudinal section showing an example of the conventional multilayer capacitor. A multilayer capacitor 51 has the ceramic sintered compact 52 constituted with the dielectric ceramics. In the ceramic sintered compact 52, it is arranged so that two or more internal electrodes 53-56 may overlap in the thickness direction through a ceramic layer. Internal electrodes 53 and 55 are pulled out by end-face 52a of the ceramic sintered compact 52, and internal electrodes 54 and 56 are pulled out by end-face 52b of the opposite side. The external electrodes 57 and 58 are formed so that end faces 52a and 52b may be covered, respectively.
[0003] In a multilayer capacitor 51, in order to carry out a surface mount to a printed circuit board etc., the external electrodes 57 and 58 have **** 57a and 58a-ed [ electrode ] which reach top-face 52c of not only a wrap but the ceramic sintered compact 52, 52d of inferior surfaces of tongue, and a both-sides side in end faces 52a and 52b.
[0004] In the multilayer capacitor 51, to make small the die length of ****-ed [ electrode ], i.e., the distance of the direction to which the end faces 52a and 52b of a sintered compact 52 are connected, with a miniaturization is tried. Therefore, in the conventional multilayer capacitor 51, distance e between the inside edge of **** 57a and 58a-ed [ electrode ] and the outermost side edge of electrodes 57 and 58 is made comparatively small. That is, distance e was made into about 1 to 1.5 times of Lg when the external electrode 58 was taken for the example, and the tips 53a and 55a of internal electrodes 53 and 55 and the external electrode 57 to which internal electrodes 53 and 55 are connected electrically set distance between the outermost side edges of the external electrode 58 of the opposite side to Lg.
[0005]
[Problem(s) to be Solved by the Invention] When it mounts a multilayer capacitor 51 in a printed circuit board by soldering etc., a thermal shock joins a multilayer capacitor 51. On the other hand, when a thermal shock is added, in the ceramic sintered compact 52, it is easy to contract the external electrodes 57 and 58 and internal electrodes 53-56 compared with the ceramics. This contraction stress tends to be concentrated on the location of the external electrodes 57 and 58 which is worn and is shown by the inside edge B of Sections 57a and 58a, for example, the arrow head of drawing 3 . Moreover, in a part for the point of internal electrodes 53-56, it is easy to produce the stress concentration by the thermal shock [ in the ceramic sintered compact 52 ]. The crack might arise between the location shown by the arrow head B which follows, for example, is shown in drawing 3 , and tip 53a of an internal electrode 53.
[0006] Moreover, after being mounted in the printed circuit board, the temperature change was given, or the printed circuit board bent, and also when the stress resulting from this deflection etc. joined the ceramic sintered compact 52, the above cracks tended to arise.
[0007] Especially, the above-mentioned distance e and distance Lg are becoming smaller with the miniaturization of a multilayer capacitor 51. Consequently, since the location shown by the arrow head B and tip 53a of an internal electrode 53 had been approaching further, there was a problem that the crack mentioned above much more became easy to happen.
[0008] Even if the purpose of this invention is the case where the temperature change was given or a substrate bends after being hard to produce the crack of a ceramic sintered compact and mounting it in a

printed circuit board etc. when the fault of the conventional technique mentioned above is canceled and a thermal shock is added like [ at the time of printed-circuit-board mounting ], it is to offer the laminating ceramic electronic parts excellent in dependability which the crack of a ceramic sintered compact cannot produce easily.

[0009]

[Means for Solving the Problem] The ceramic sintered compact which has the 1st and 2nd end face which the laminating ceramic electronic parts concerning this invention counter for each other, Two or more internal electrodes which are arranged so that it may overlap in the thickness direction through a ceramic layer in said ceramic sintered compact, and were pulled out by the 1st or 2nd end face, It has the 1st and 2nd external electrode formed so that the 1st and 2nd end face which said ceramic sintered compact counters for each other might be covered, respectively. It has ****-ed [ electrode ] to which the said 1st and 2nd external electrode reaches not only the 1st or 2nd end face of a ceramic sintered compact but a top face, an inferior surface of tongue, and a both-sides side. The outermost side edge of an external electrode, When distance between the inside edges of ****-ed [ electrode ] of this external electrode is set to e and distance between the outermost side edge of this external electrode and the tip of the internal electrode electrically connected to the external electrode of the opposite side is set to Lg, it is characterized by being constituted so that 1.5xLg<=e<=3.5xLg may be filled.

[0010] Preferably, distance e and distance Lg are constituted so that 2.0xLg<=e<=3.5xLg may be filled. Although the laminating ceramic electronic parts concerning this invention can be applied to various laminating ceramic electronic parts, such as a multilayer capacitor, a laminating varistor, and a laminating thermistor, the dielectric ceramics is used as the above-mentioned ceramic sintered compact, and a multilayer capacitor is constituted from a specific aspect of affairs of this invention by it.

[0011]

[Embodiment of the Invention] Hereafter, this invention is clarified by explaining the concrete example of this invention, referring to a drawing.

[0012] Drawing 1 is the sectional view showing the multilayer capacitor as laminating ceramic electronic parts concerning one example of this invention, and drawing 2 is the perspective view showing the appearance. A multilayer capacitor 1 has the ceramic sintered compact 2 of the shape of a rectangular parallelepiped which consists of dielectric ceramics like barium titanate series ceramics.

[0013] In the ceramic sintered compact 2, it is arranged so that two or more internal electrodes 3-6 may overlap in the thickness direction through a ceramic layer. Internal electrodes 3-6 are constituted by metallic materials, such as Ag, Ag-Pd, and nickel.

[0014] Internal electrodes 3 and 5 are pulled out by 1st end-face 2a of the ceramic sintered compact 2, and another side and internal electrodes 4 and 6 are pulled out by the 1st end face and 2nd end-face 2b which has countered.

[0015] The 1st external electrode 7 is formed so that end-face 2a may be covered, and the 1st external electrode 7 is electrically connected to internal electrodes 3 and 5. The external electrode 7 is formed so that end-face 2a may be resulted in side-face 2of top-faces [ of not only a wrap but the ceramic sintered compact 2 ]c [ 2 ] and 2d, and pair e (not shown [ the side face of the other side ]). That is, the external electrode 7 has ****-ed [ electrode ] 7a which results in side-face 2of top-face 2c [ of the ceramic sintered compact 2 ], 2d [ of inferior surfaces of tongue ], and pair e like the case of the conventional multilayer capacitor 51.

[0016] Similarly, the 2nd external electrode 8 has ****-ed [ electrode ] 8a which is formed so that end-face 2b of the ceramic sintered compact 2 may be covered, and results in side-face 2of top-face 2c [ of the ceramic sintered compact 2 ], 2d [ of inferior surfaces of tongue ], and pair e.

[0017] The distance e mentioned above and distance Lg have the description of the multilayer capacitor 1 of this example in being constituted so that 1.5xLg<=e<=3.5xLg may be filled. This is explained taking the case of the 2nd external electrode 8.

[0018] As shown in drawing 1 , distance e is the distance between the outermost side edge of the 2nd external electrode 8, and the inside edge of ****-ed [ electrode ] 8a. In addition, let the direction which goes the direction of the interior of a ceramic sintered compact to the inside and an outside from end-face 2b be an outside in end-face 2b in which the external electrode 8 is formed.

[0019] Moreover, the distance between the outermost side edge of the 2nd external electrode 8 and the tips 3a and 5a of the internal electrodes 3 and 5 electrically connected to the 1st external electrode 7 is said in distance Lg. In addition, it is constituted so that the relation which distance e and distance Lg mentioned above similarly to the 1st external electrode 7 side may be filled.

[0020] Moreover, the external electrodes 7 and 8 may be the structures which carried out the laminating

of two or more metal layers, and the outermost side edge of the maximum outside layer will constitute the above-mentioned outermost side edge in that case. Since it is constituted so that distance e and distance Lg may fill the above-mentioned relation with the multilayer capacitor 1 of this example, stress concentration the case where the external force resulting from the deflection of the substrate at the time of substrate mounting joins the ceramic sintered compact 2, and when the stress resulting from a thermal shock is added is eased, it bends by it, and the fall of a property and generating of the crack by the thermal shock can be controlled. This is explained based on the concrete example of an experiment.

[0021] The ceramic green sheet of the mother by whom thickness was set up so that it might roast and next thickness might be set to about 8 micrometers was prepared. Since an internal electrode was constituted on the top face of this mother's ceramic green sheet, conductive paste was screen-stenciled.

[0022] The 70-sheet laminating of the ceramic green sheet with which conductive paste was printed was carried out, the laminating of every 30 plain ceramic green sheets was carried out up and down, and the layered product was obtained. After pressurizing this layered product in the thickness direction, it cut in the thickness direction and the layered product of each multilayer capacitor unit was obtained.

[0023] After an appropriate time, the above-mentioned layered product was calcinated and the ceramic sintered compact 2 was obtained. Ag paste was applied, by the ability being burned, the 1st external electrode layer was formed in the both-ends side of the ceramic sintered compact 2, further, nickel plating layer and Sn plating layer were formed in that outside front face in this sequence, and the 1st and 2nd external electrode 7 and 8 was formed in it. The multilayer capacitor of the dimension of the 1.0mm of the die-length [ of 2.0mm ] x width-of-face [ of 1.25mm ] x thickness directions was obtained as mentioned above.

[0024] Moreover, in obtaining the above-mentioned multilayer capacitor, distance Lg was set to 0.35mm, distance e was changed variously, and each multilayer capacitor of sample numbers 1-6 shown in the following table 1 was obtained. About each multilayer capacitor of the sample numbers 1-6 obtained as mentioned above, the flexure test and the spalling test were performed in the following ways.

[0025] ** Flexure test -- JIS The amount of marginal deflections was measured according to C-5102-1994, and 8, 11 and 1, and it considered as the deflection force. It is shown that a multilayer capacitor can bear to the big deflection force, so that this deflection force is large.

[0026] ** Spalling test -- JIS According to C-5102-1994, and 8 and 14, the spalling test was performed for the multilayer capacitor using melting solder with a temperature of 300 degrees C. In this case, the existence of generating of the crack in the multilayer capacitor after a spalling test was checked.

[0027] A result is shown in the following table 1.

[0028]

[Table 1]

| 試料番号 | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| 距離e | 1.2 ×Lg | 1.6 ×Lg | 2.3 ×Lg | 3.0 ×Lg | 3.5 ×Lg | 4.0 ×Lg |
| たわみ力〔mm〕（min値） | 2.8 (2.2) | 3.8 (2.8) | 4.7 (3.5) | 4.9 (3.8) | 5.1 (4.2) | 4.8 |
| はんだ耐熱性クラック発生数 | 45/200 | 2/200 | 0/200 | 0/200 | 0/200 | 0/200 |

[0029] The sample numbers 2-5 included in the range of this invention showed the good result also in any of a flexure test and a spalling test so that clearly from Table 1. That is, the big deflection force was borne and the generating rate of a crack was very low in the spalling test.

[0030] On the other hand, in the multilayer capacitor of the sample number 1 smaller than 1.5Lg, the deflection force had a small distance e, and the crack had occurred in many multilayer capacitors in the spalling test.

[0031] Moreover, when distance e will exceed 3.5Lg(s) so that clearly if the result of sample numbers 5 and 6 is compared, it turns out that a deflection property deteriorates. moreover, clear from sample numbers 3-5 -- as -- distance e -- more than 2.0xLg -- the case below 3.5xLg -- a deflection property and its heat-resistant any -- although -- it turns out that it is much more good.

[0032]

[Effect of the Invention] In the laminating ceramic electronic parts concerning this invention, the outermost side edge of an external electrode, When distance between the inside edges of ****-ed [ electrode ] of an external electrode is set to e and distance between the outermost side edge of this external electrode and the tip of the internal electrode electrically connected to the external electrode of

the opposite side is set to Lg Since it is referred to as 1.5xLg<=e<=3.5xLg, even if the stress resulting from the deflection of the substrate at the time of mounting laminating ceramic electronic parts in a substrate is added, the stress concentration in laminating ceramic electronic parts can be eased. Similarly, even if a thermal shock is added like at the time of soldering, the stress concentration resulting from this thermal shock is also eased. Therefore, the crack of a ceramic sintered compact can be controlled effectively and it becomes possible to offer laminating ceramic electronic parts excellent in dependability.

[0033] In the case of small laminating ceramic electronic parts, the crack of the ceramic sintered compact resulting from the above-mentioned stress concentration tends to arise especially, but according to this invention, even if it is the case where a miniaturization is advanced, the above-mentioned crack of a ceramic sintered compact can be controlled effectively. It follows, for example, is 1.0mm or less in die-length [ of 2mm ] x width-of-face [ of 1.25mm ] x thickness, and 100 or more layers, when an internal electrode number of layers applies to small and the mass multilayer capacitor of 50 or more layers further by 0.5mm or less in die-length [ of 1mm ] x width-of-face [ of 0.5mm ] x thickness, especially the effectiveness of this invention has the large number of internal electrode laminatings.
[0034] In this invention, when referred to as 2.0xLg<=e<=3.5xLg, the stress concentration in a ceramic sintered compact can be eased further, and generating of the crack in a ceramic sintered compact can be more effectively controlled so that clearly from the example of an experiment mentioned above.
[0035] Therefore, when a multilayer capacitor is constituted using the dielectric ceramics as a ceramic sintered compact, generating of the crack of the ceramic sintered compact at the time of mounting in a printed circuit board etc. or the time of use can be controlled effectively, and it becomes possible to offer the multilayer capacitor excellent in dependability.

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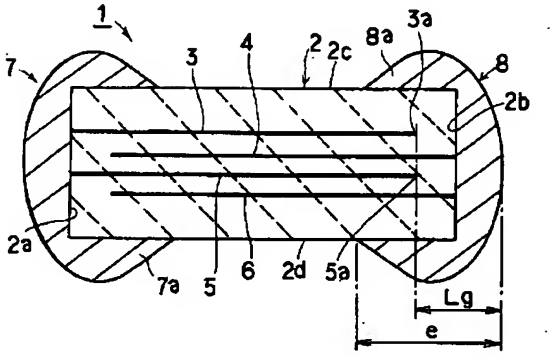
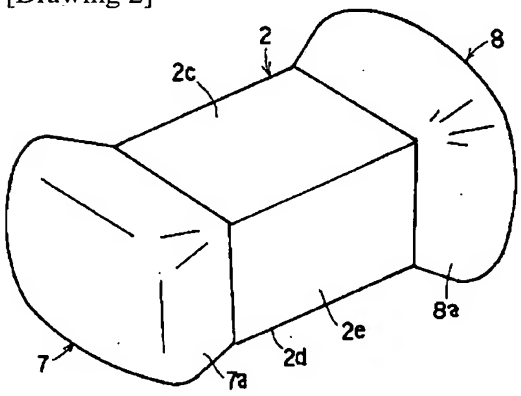
## DRAWINGS

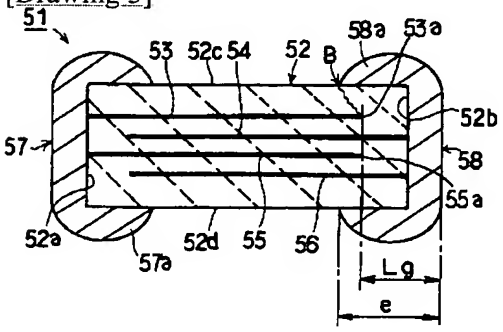
[Drawing 1]




[Drawing 2]




[Drawing 3]

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審査請求　未請求　請求項の数３　ＯＬ　（全　５　頁）

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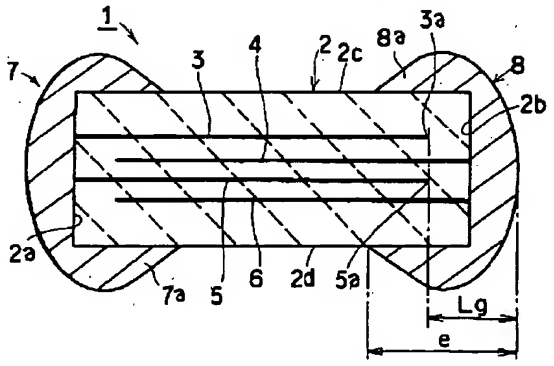
最終頁に続く

(54)【発明の名称】　積層セラミック電子部品

(57)【要約】
【課題】　熱衝撃が加えられた場合や実装後のプリント回路基板のたわみに起因する応力が加わった場合であっても、セラミック焼結体のクラックが生じ難い、信頼性に優れた積層セラミック電子部品を得る。
【解決手段】　セラミック焼結体２内に内部電極３～６が配置されており、第１，第２の端面２ａ，２ｂを覆うように第１，第２の外部電極７，８が形成されており、第１，第２の外部電極７，８が、セラミック焼結体の上面２ｃ、下面２ｃ及び両側面に至る電極被り部７ａ，８ａを有し、外部電極７，８の最外側端と、外部電極７，８の電極被り部７ａ，８ａの内側端との間の距離をｅ、外部電極７，８の最外側端と、反対側の外部電極８，７に電気的に接続される内部電極の先端との間の距離をＬｇとしたときに、１．５×Ｌｇ≦ｅ≦３．５×Ｌｇとされている、積層セラミック電子部品。



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【特許請求の範囲】

【請求項１】　対向し合う第１，第２の端面を有するセラミック焼結体と、

前記セラミック焼結体内においてセラミック層を介して厚み方向に重なり合うように配置されており、かつ第１または第２の端面に引き出された複数の内部電極と、

前記セラミック焼結体の対向し合う第１，第２の端面をそれぞれ覆うように形成された第１，第２の外部電極とを備え、

前記第１，第２の外部電極が、セラミック焼結体の第１または第２の端面だけでなく、上面、下面及び両側面に至る電極被り部を有し、

外部電極の最外側端と、該外部電極の電極被り部の内側端との間の距離をｅとし、該外部電極の最外側端と、反対側の外部電極に電気的に接続されている内部電極の先端との間の距離をＬｇとしたときに、１．５×Ｌｇ≦ｅ≦３．５×Ｌｇを満たすように構成されていることを特徴とする、積層セラミック電子部品。

【請求項２】　距離ｅ及び距離Ｌｇが、２．０×Ｌｇ≦ｅ≦３．５×Ｌｇを満たすように構成されている、請求項１に記載の積層セラミック電子部品。

【請求項３】　前記セラミック焼結体が誘電体セラミックスを用いて構成されており、それによって積層コンデンサとされている、請求項１または２に記載の積層セラミック電子部品。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、例えば積層コンデンサや積層バリスタなどの積層セラミック電子部品に関し、より詳細には、電極構造が改良された積層セラミック電子部品に関する。

【０００２】

【従来の技術】図３は、従来の積層コンデンサの一例を示す縦断面図である。積層コンデンサ５１は、誘電体セラミックスにより構成されたセラミック焼結体５２を有する。セラミック焼結体５２内には、複数の内部電極５３～５６がセラミック層を介して厚み方向に重なり合うように配置されている。内部電極５３，５５は、セラミック焼結体５２の端面５２ａに引き出されており、内部電極５４，５６は反対側の端面５２ｂに引き出されている。端面５２ａ，５２ｂをそれぞれ覆うように、外部電極５７，５８が形成されている。

【０００３】積層コンデンサ５１では、プリント回路基板などに表面実装するために、外部電極５７，５８は、端面５２ａ，５２ｂを覆うだけでなく、セラミック焼結体５２の上面５２ｃ，下面５２ｄ及び両側面に至る電極被り部５７ａ，５８ａを有する。

【０００４】積層コンデンサ５１では、小型化にともない、電極被り部の長さ、すなわち焼結体５２の端面５２ａ，５２ｂを結ぶ方向の距離を小さくすることが試みられている。従って、従来の積層コンデンサ５１では、電極被り部５７ａ，５８ａの内側端と、電極５７，５８の最外側端との間の距離ｅが比較的小さくされている。すなわち、外部電極５８を例にとると、内部電極５３，５５の先端５３ａ，５５ａと、内部電極５３，５５が電気的に接続される外部電極５７とは反対側の外部電極５８の最外側端との間の距離をＬｇとしたときに、距離ｅはＬｇの１～１．５倍程度にされていた。

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【０００５】

【発明が解決しようとする課題】積層コンデンサ５１をプリント回路基板に半田付け等により実装する場合、積層コンデンサ５１には熱衝撃が加わる。他方、熱衝撃が加わった場合、セラミック焼結体５２においては、外部電極５７，５８や内部電極５３～５６がセラミックスに比べて収縮し易い。この収縮応力は、外部電極５７，５８の被り部５７ａ，５８ａの内側端、例えば図３の矢印Ｂで示す位置に集中しがちである。また、セラミック焼結体５２内においては、内部電極５３～５６の先端部分において、熱衝撃による応力集中が生じ易い。従って、例えば、図３に示す矢印Ｂで示す位置と、内部電極５３の先端５３ａとの間でクラックが生じることがあった。

【０００６】また、プリント回路基板に実装された後、温度変化が与えられたり、プリント回路基板がたわんだりし、セラミック焼結体５２に該たわみ等に起因する応力が加わった場合にも、上記のようなクラックが生じがちであった。

【０００７】特に、積層コンデンサ５１の小型化に伴って、上記距離ｅや距離Ｌｇはより小さくなってきている。その結果、矢印Ｂで示す位置と、内部電極５３の先端５３ａとがより一層近づいてきているので、上述したクラックがより一層起こり易くなるという問題があった。

【０００８】本発明の目的は、上述した従来技術の欠点を解消し、プリント回路基板実装時のように熱衝撃が加えられた場合にセラミック焼結体のクラックが生じ難く、かつプリント回路基板などに実装された後に温度変化が与えられたり、基板がたわんだりした場合であってもセラミック焼結体のクラックが生じ難い、信頼性に優れた積層セラミック電子部品を提供することにある。

【０００９】

【課題を解決するための手段】本発明に係る積層セラミック電子部品は、対向し合う第１，第２の端面を有するセラミック焼結体と、前記セラミック焼結体内においてセラミック層を介して厚み方向に重なり合うように配置されており、かつ第１または第２の端面に引き出された複数の内部電極と、前記セラミック焼結体の対向し合う第１，第２の端面をそれぞれ覆うように形成された第１，第２の外部電極とを備え、前記第１，第２の外部電極が、セラミック焼結体の第１または第２の端面だけでなく、上面、下面及び両側面に至る電極被り部を有し、

外部電極の最外側端と、該外部電極の電極被り部の内側端との間の距離をｅとし、該外部電極の最外側端と、反対側の外部電極に電気的に接続されている内部電極の先端との間の距離をＬｇとしたときに、１．５×Ｌｇ≦ｅ≦３．５×Ｌｇを満たすように構成されていることを特徴とする。

【００１０】好ましくは、距離ｅ及び距離Ｌｇが、２．０×Ｌｇ≦ｅ≦３．５×Ｌｇを満たすように構成されている。本発明に係る積層セラミック電子部品は、積層コンデンサ、積層バリスタ、積層サーミスタなどの様々な積層セラミック電子部品に適用し得るが、本発明の特定の局面では、上記セラミック焼結体として誘電体セラミックスが用いられ、それによって積層コンデンサが構成される。

【００１１】

【発明の実施の形態】以下、図面を参照しつつ本発明の具体的な実施例を説明することにより、本発明を明らかにする。

【００１２】図１は、本発明の一実施例に係る積層セラミック電子部品としての積層コンデンサを示す断面図であり、図２はその外観を示す斜視図である。積層コンデンサ１は、例えばチタン酸バリウム系セラミックスのような誘電体セラミックスよりなる直方体状のセラミック焼結体２を有する。

【００１３】セラミック焼結体２内には、複数の内部電極３～６がセラミック層を介して厚み方向に重なり合うように配置されている。内部電極３～６は、例えばＡｇ、Ａｇ－Ｐｄ、Ｎｉなどの金属材料により構成される。

【００１４】内部電極３，５は、セラミック焼結体２の第１の端面２ａに引き出されており、他方、内部電極４，６は、第１の端面と対向している第２の端面２ｂに引き出されている。

【００１５】端面２ａを覆うように第１の外部電極７が形成されており、第１の外部電極７は、内部電極３，５に電気的に接続されている。外部電極７は、端面２ａを覆うだけでなく、セラミック焼結体２の上面２ｃ、２ｄ及び一対の側面２ｅ（他方側の側面は図示されず）に至るように形成されている。すなわち、従来の積層コンデンサ５１の場合と同様に、外部電極７は、セラミック焼結体２の上面２ｃ、下面２ｄ及び一対の側面２ｅに至る電極被り部７ａを有する。

【００１６】同様に、第２の外部電極８は、セラミック焼結体２の端面２ｂを覆うように形成されており、かつセラミック焼結体２の上面２ｃ、下面２ｄ及び一対の側面２ｅに至る電極被り部８ａを有する。

【００１７】本実施例の積層コンデンサ１の特徴は、前述した距離ｅ及び距離Ｌｇが、１．５×Ｌｇ≦ｅ≦３．５×Ｌｇを満たすように構成されていることにある。これを、第２の外部電極８を例にとり説明する。

【００１８】図１に示すように、距離ｅは、第２の外部電極８の最外側端と、電極被り部８ａの内側端との間の距離である。なお、外部電極８が形成されている端面２ｂにおいて、セラミック焼結体内部方向を内側、端面２ｂから外側に向かう方向を外側とする。

【００１９】また、距離Ｌｇとは、第２の外部電極８の最外側端と、第１の外部電極７に電気的に接続されている内部電極３，５の先端３ａ，５ａとの間の距離をいう。なお、第１の外部電極７側においても、同様に、距離ｅと距離Ｌｇとが上述した関係を満たすように構成されている。

【００２０】また、外部電極７，８は、複数の金属層を積層した構造であってもよく、その場合においては、最外側層の最外側端が上記最外側端を構成することになる。本実施例の積層コンデンサ１では、距離ｅ及び距離Ｌｇが上記関係を満たすように構成されているので、基板実装時の基板のたわみに起因する外力がセラミック焼結体２に加わった場合や、熱衝撃に起因する応力が加わった場合の応力集中が緩和され、それによってたわみ特性の低下や熱衝撃によるクラックの発生を抑制することができる。これを、具体的な実験例に基づき説明する。

【００２１】焼き上げ後の厚みが約８μｍとなるように厚みが設定されたマザーのセラミックグリーンシートを用意した。このマザーのセラミックグリーンシートの上面に、内部電極を構成するために導電ペーストをスクリーン印刷した。

【００２２】導電ペーストが印刷されたセラミックグリーンシートを７０枚積層し、上下に無地のセラミックグリーンシートを３０枚ずつ積層し、積層体を得た。この積層体を厚み方向に加圧した後、厚み方向に切断し、個々の積層コンデンサ単位の積層体を得た。

【００２３】しかる後、上記積層体を焼成し、セラミック焼結体２を得た。セラミック焼結体２の両端面に、Ａｇペーストを塗布し、焼き付けることにより、第１の外部電極層を形成し、さらにその外側表面に、Ｎｉめっき層及びＳｎめっき層をこの順序で形成して、第１，第２の外部電極７，８を形成した。上記のようにして、長さ２．０ｍｍ×幅１．２５ｍｍ×厚み方向１．０ｍｍの寸法の積層コンデンサを得た。

【００２４】また、上記積層コンデンサを得るにあたり、距離Ｌｇを０．３５ｍｍとし、距離ｅを種々異ならせ、下記の表１に示す試料番号１～６の各積層コンデンサを得た。上記のようにして得た試料番号１～６の各積層コンデンサについて、たわみ試験及び熱衝撃試験を以下の要領で行った。

【００２５】①たわみ試験…ＪＩＳ　Ｃ－５１０２－１９９４、８、１１、１に従って限界たわみ量を測定し、たわみ力とした。このたわみ力が大きい程、積層コンデンサが大きなたわみ力に対して耐え得ることを示す。

【００２６】②熱衝撃試験…ＪＩＳ　Ｃ－５１０２－１

９９４、８、１４に従って積層コンデンサを３００℃の温度の溶融半田を用いて熱衝撃試験を行った。この場合、熱衝撃試験後の積層コンデンサにおけるクラックの発生の有無を確認した。



＊【００２７】結果を下記の表１に示す。

【００２８】

【表１】

＊

| 試料番号 | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| 距離ｅ | 1.2 ×Lg | 1.6 ×Lg | 2.3 ×Lg | 3.0 ×Lg | 3.5 ×Lg | 4.0 ×Lg |
| たわみ力〔mm〕（ｍｉｎ値） | 2.8 (2.2) | 3.8 (2.8) | 4.7 (3.5) | 4.9 (3.8) | 5.1 (4.2) | 4.8 |
| はんだ耐熱性クラック発生数 | 45/200 | 2/200 | 0/200 | 0/200 | 0/200 | 0/200 |

【００２９】表１から明らかなように、本発明の範囲に入る試料番号２～５では、たわみ試験及び熱衝撃試験のいずれにおいても良好な結果を示した。すなわち、大きなたわみ力に耐え、かつ熱衝撃試験においてクラックの発生割合が非常に低かった。

【００３０】これに対して、距離ｅが、１．５Ｌｇより小さい試料番号１の積層コンデンサでは、たわみ力が小さく、かつ熱衝撃試験において多数の積層コンデンサにクラックが発生していた。

【００３１】また、試料番号５と６の結果を比較すれば明らかなように、距離ｅが３．５Ｌｇを超えると、たわみ特性の劣化することがわかる。また、試料番号３～５から明らかなように、距離ｅが、２．０×Ｌｇ以上、３．５×Ｌｇ以下の場合、たわみ特性及びその耐熱性のいずれもがより一層良好であることがわかる。

【００３２】

【発明の効果】本発明に係る積層セラミック電子部品では、外部電極の最外側端と、外部電極の電極被り部の内側端との間の距離をｅとし、該外部電極の最外側端と、反対側の外部電極に電気的に接続されている内部電極の先端との間の距離をＬｇとしたときに、１．５×Ｌｇ≦ｅ≦３．５×Ｌｇとされているので、積層セラミック電子部品を基板に実装した際の基板のたわみに起因する応力が加わったとしても、積層セラミック電子部品における応力集中を緩和することができる。同様に、半田付け時等のように熱衝撃が加わったとしても、該熱衝撃に起因する応力集中も緩和される。よって、セラミック焼結体のクラックを効果的に抑制することができ、信頼性に優れた積層セラミック電子部品を提供することが可能となる。

【００３３】特に、小型の積層セラミック電子部品の場合には、上記応力集中に起因するセラミック焼結体のクラックが生じがちであるが、本発明によれば、小型化を進めた場合であっても、セラミック焼結体の上記クラックを効果的に抑制することができる。従って、例えば、長さ２ｍｍ×幅１．２５ｍｍ×厚さ１．０ｍｍ以下であり内部電極積層数が１００層以上、さらに長さ１ｍｍ×幅０．５ｍｍ×厚さ０．５ｍｍ以下で内部電極層数が５０層以上の小型・大容量の積層コンデンサに適用した場合、本発明の効果は特に大きい。

【００３４】本発明において、２．０×Ｌｇ≦ｅ≦３．５×Ｌｇとされている場合には、上述した実験例から明らかなように、セラミック焼結体における応力集中をより一層緩和することができ、セラミック焼結体におけるクラックの発生をより効果的に抑制することができる。

【００３５】従って、セラミック焼結体として誘電体セラミックスを用い、積層コンデンサを構成した場合、プリント回路基板などに実装する際や使用時におけるセラミック焼結体のクラックの発生を効果的に抑制することができ、信頼性に優れた積層コンデンサを提供することが可能となる。

【図面の簡単な説明】

【図１】本発明の一実施例に係る積層セラミック電子部品としての積層コンデンサを示す縦断面図。

【図２】図１に示した実施例の積層コンデンサの外観を示す斜視図。

【図３】従来の積層コンデンサを示す縦断面図。

【符号の説明】

１…積層コンデンサ

２…セラミック焼結体

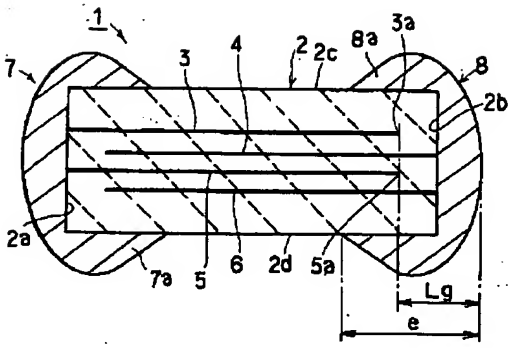
２ａ，２ｂ…第１，第２の端面

３～６…内部電極

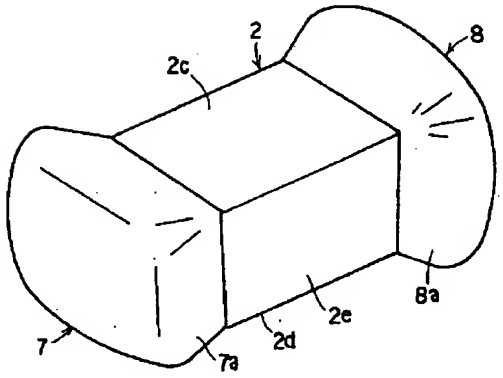
７，８…第１，第２の外部電極

７ａ，８ａ…電極被り部

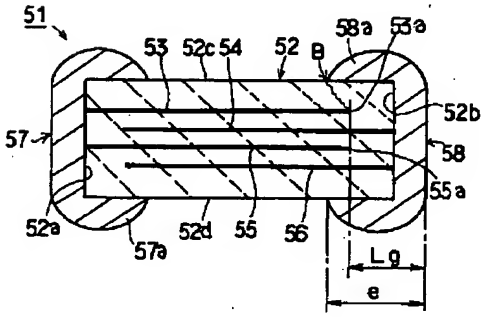
【図１】




【図２】




【図３】

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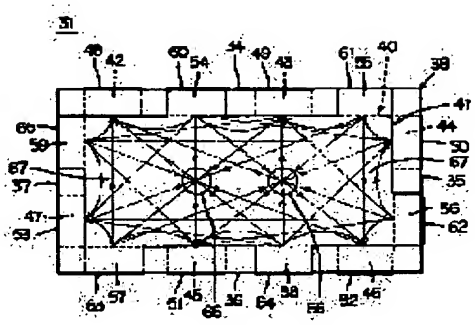
## (54) LAMINATED CAPACITOR

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce an equivalent series inductance of a laminated capacitor.

SOLUTION: Lead-out electrodes 42-47, 54-59 of internal electrodes 40 and 41 are led out above four side surfaces 34-37 of a capacitor main body 38, respectively, and external terminal electrodes 48-53, 60-65 connected electrically to the lead-out electrodes 42-47, 54-59, respectively, are provided on the four side surfaces 34-37. Here, external terminal electrodes connected to different internal electrodes are so provided as to be adjacent to each other alternately. In this way, the currents flowing in the internal electrodes 40 and 41 are diverged respectively, so that the magnetic flux which is produced related to a current is canceled to reduce an equivalent series inductance.



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* NOTICES *



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2.**** shows the word which can not be translated.
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## CLAIMS

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[Claim(s)]
[Claim 1] It has the body of a capacitor of the shape of a rectangular parallelepiped which has four side faces which connect between two principal planes which carry out phase opposite, and these principal planes. Said body of a capacitor It has two or more dielectric layers prolonged in the direction of said principal plane, and at least one pair of 1st and 2nd internal electrodes which counter mutually through said specific dielectric layer so that a capacitor unit may be formed. The drawer electrode pulled out even upwards is formed. said 1st and 2nd internal electrodes -- respectively -- either of said side faces -- at least one side of said 1st and 2nd internal electrodes As said drawer electrode, at least three drawer electrodes of said at least three side faces pulled out even upwards, respectively are respectively formed among said four side faces. The multilayer capacitor with which the external terminal electrode of said side face in which said drawer electrode was pulled out electrically connected to said drawer electrode upwards is prepared, respectively.
[Claim 2] Said 1st internal electrode forms respectively 1st at least three drawer electrode of said at least three side faces pulled out even upwards, respectively among said four side faces as said drawer electrode. Said at least three side faces in which said 1st drawer electrode was pulled out respectively upwards The 1st external terminal electrode electrically connected to said 1st drawer electrode as said external terminal electrode is prepared, respectively. Said 2nd internal electrode As said drawer electrode, 2nd at least three drawer electrode of said at least three side faces pulled out even upwards, respectively is respectively formed among said four side faces. In a different location from the location in which said at least three side faces in which said 2nd drawer electrode was pulled out are tops respectively, and said 1st external terminal electrode was prepared The multilayer capacitor according to claim 1 with which the 2nd external terminal electrode electrically connected to said 2nd drawer electrode as said external terminal electrode is prepared, respectively.
[Claim 3] Said 1st external terminal electrode is a multilayer capacitor of said four side faces in which said 1st internal electrode formed said 1st at least four drawer electrode of said four side faces pulled out even upwards, respectively, and said 1st drawer electrode was pulled out according to claim 2 formed upwards respectively.
[Claim 4] Said 2nd external terminal electrode is a multilayer capacitor of said four side faces in which said 2nd internal electrode formed said 2nd at least four drawer electrode of said four side faces pulled out even upwards, respectively, and said 2nd drawer electrode was pulled out according to claim 2 or 3 formed upwards respectively.
[Claim 5] Said all 1st external terminal electrode is a multilayer capacitor according to claim 2 to 4 arranged so that said 2nd external terminal electrode may be adjoined on each aforementioned side face in which the 1st external terminal electrode concerned was prepared.
[Claim 6] Said all 1st external terminal electrode and said all 2nd external terminal electrode are a multilayer capacitor according to claim 5 arranged by turns through said four side faces.
[Claim 7] It is the multilayer capacitor according to claim 1 to 6 with which the number of the parts of said 1st internal electrode and said 2nd internal electrode which counter is made into plurality so that said two or more capacitor units in which parallel connection was carried out by at least one side of said 1st and 2nd external terminal electrodes may be formed.
[Claim 8] Said one [ at least ] drawer electrode of said 1st and 2nd internal electrodes is a multilayer capacitor according to claim 1 to 7 currently pulled out by at least two on said at least one side face.
[Claim 9] It has further the 3rd internal electrode which counters through said specific dielectric layer at least to one side of said 1st and 2nd internal electrodes. Said 3rd internal electrode Said side face in which

formed 3rd at least two drawer electrode of said at least two side faces pulled out even upwards, respectively, and said 3rd drawer electrode was pulled out respectively upwards The multilayer capacitor according to claim 1 to 8 with which the 3rd external terminal electrode electrically connected to said 3rd drawer electrode is prepared, respectively.

[Claim 10] Said all 1st external terminal electrode, said all 2nd external terminal electrode, and said all 3rd external terminal electrode are a multilayer capacitor according to claim 9 arranged while repeating the same array sequence through said four side faces.

[Claim 11] For the external terminal electrode which makes common said internal electrode connected to this, said all external terminal electrodes are multilayer capacitors according to claim 1 to 10 arranged so that each other may not be adjoined.

[Claim 12] Said external terminal electrode is a multilayer capacitor of said four side faces according to claim 1 to 11 formed upwards, respectively.

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[Translation done.]

## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the multilayer capacitor which may be especially applied advantageously in a high frequency circuit about a multilayer capacitor.
[0002]
[Description of the Prior Art] There are some which were indicated by JP,2-256216,A as a conventional multilayer capacitor interesting for this invention. Here, the multilayer capacitor 1 as shown in drawing 15 thru/or drawing 17 is indicated. Drawing 15 is the top view showing the appearance of a multilayer capacitor 1, drawing 16 is the top view in which having the 1st cross section and showing the internal structure of a multilayer capacitor 1, and drawing 17 is the top view showing the internal structure of a multilayer capacitor 1 with the 2nd cross section where the 1st cross sections differ.
[0003] The multilayer capacitor 1 is equipped with the body 8 of a capacitor of the shape of a rectangular parallelepiped which has four side faces 4, 5, 6, and 7 which connect between two principal planes 2 and 3 which carry out phase opposite, these principal planes 2, and 3 as the appearance is shown in drawing 15 . The body 8 of a capacitor was prolonged in the direction of principal planes 2 and 3, for example, is equipped with two or more dielectric layers 9 which consist of a ceramic dielectric, and at least one pair of 1st and 2nd internal electrodes 10 and 11 which counter mutually through the specific dielectric layer 9 so that a capacitor unit may be formed.
[0004] Drawing 16 shows the cross section along which the 1st internal electrode 10 passes as the 1st internal electrode 10 is shown in drawing 16 . Moreover, drawing 17 shows the cross section along which the 2nd internal electrode 11 passes as the 2nd internal electrode 11 is shown in drawing 17 . Reduction-ization of an equivalence serial inductance (ESL) is attained so that this multilayer capacitor 1 may fit use in a RF region.
[0005] Therefore, the 1st internal electrode 10 forms respectively the 1st four drawer electrode 12, 13, 14, and 15 of two side faces 4 and 6 which carry out phase opposite pulled out upwards, respectively. More, the drawer electrodes 12 and 13 are pulled out even on a side face 4, and the drawer electrodes 14 and 15 are pulled out by the detail even on the side face 6. Moreover, the 1st external terminal electrode 16, 17, 18, and 19 of the side faces 4 and 6 in which the 1st above-mentioned drawer electrode 12-15 was pulled out electrically connected to the drawer electrodes 12-15 of these 1st upwards is formed, respectively. That is, the external terminal electrodes 16 and 17 are connected to the drawer electrodes 12 and 13 on a side face 4, respectively, and the external terminal electrodes 18 and 19 are connected to the drawer electrodes 14 and 15 on the side face 6, respectively.
[0006] On the other hand, the 2nd internal electrode 11 forms respectively the 2nd four drawer electrode 20, 21, 22, and 23 of two side faces 4 and 6 which carry out phase opposite pulled out upwards, respectively. It is pulled out by even different location from the location where the 1st drawer electrode 14 and 15 which the location where the 1st drawer electrode 12 and 13 which the drawer electrodes 20 and 21 are on a side face 4, and was mentioned above at the detail was pulled out is pulled out by even different location, and the drawer electrodes 22 and 23 are on a side face 6 more, and was mentioned above was pulled out.
[0007] Moreover, the 2nd external terminal electrode 24, 25, 26, and 27 of the side faces 4 and 6 in which the 2nd above-mentioned drawer electrode 20-23 was pulled out electrically connected to the drawer electrodes 20-23 of these 2nd upwards is formed, respectively. That is, external terminal electrodes 24 and 25 are connected to the drawer electrodes 20 and 21 on a side face 4, respectively in a different location from the location in which the 1st external terminal electrode 16 and 17 mentioned above was formed,

and external terminal electrodes 26 and 27 are connected to drawer electrodes 22 and 23 on a side face 6, respectively in a different location from the location in which the 1st external terminal electrode 18 and 19 mentioned above was formed.

[0008] Thus, if it is on two side faces 4 and 6, it is arranged so that two or more 1st external terminal electrodes 16-19 and two or more 2nd external terminal electrodes 24-27 may adjoin each other by turns.

[0009]

[Problem(s) to be Solved by the Invention] The current which flows in this multilayer capacitor 1 is shown in drawing 18 in illustration with the top view equivalent to drawing 17 . In drawing 18 , the 1st internal electrode 10 is shown by the broken line, and the 2nd internal electrode 11 is shown by the continuous line, and after these have piled up, it is illustrated.

[0010] In drawing 18 , the typical path and typical direction of a current are shown by the arrow head. As shown by these arrow heads, the current shall flow toward each of the 1st external terminal electrode 16-19 from each of the 2nd external terminal electrode 24-27 at the illustrated condition or the time. In addition, also when flowing conversely with a natural thing in an alternating current, it is.

[0011] When a current flows, induction of the magnetic flux it is decided in the direction of a current that the direction will be is carried out as everyone knows, therefore a self-inductance component arises. In drawing 18 , in the center section 28 of the internal electrodes 10 and 11 shown by O, since a current flows in the various directions and the magnetic flux in which induction is carried out by the current is offset, there is almost no generating of magnetic flux.

[0012] Moreover, although a current is in the inclination which separates from each of the 2nd external terminal electrode 24-27 toward each of the 1st external terminal electrode 16-19 the external terminal electrodes 16-19 and near 24-27, the current which flows leftward by drawing 18 with the breadth of 180 abbreviation, and the current which flows rightward exist. Therefore, the most is offset, consequently magnetic flux does not bring about generating of serious magnetic flux.

[0013] Therefore, in the point which mentioned above the multilayer capacitor 1 shown in drawing 15 thru/or drawing 17 , generating of a self-inductance is controlled and low ESL-ization is attained. However, in each edge 29 of the right and left which performed and showed hatching [ near / each / the side faces 5 and 7 in which any external terminal electrode is not located (i.e. drawing 18 ) ], since a current flows in the almost fixed direction, it was not generated substantially but offset of magnetic flux has brought about generating and increase of a self-inductance to the last.

[0014] Therefore, the cure for the reduction in ESL attained in the multilayer capacitor 1 shown in drawing 15 thru/or drawing 17 can be said to be still inadequate in the point of effectiveness. Then, the purpose of this invention is offering the multilayer capacitor improved so that low ESL-ization could be attained more effectively.

[0015]

[Means for Solving the Problem] The multilayer capacitor concerning this invention is equipped with the body of a capacitor of the shape of a rectangular parallelepiped which has four side faces which connect between two principal planes which carry out phase opposite, and these principal planes. moreover, at least one pair of 1st and 2nd internal electrodes which counter mutually through a specific dielectric layer so that this body of a capacitor may form two or more dielectric layers prolonged in the direction of a principal plane, and a capacitor unit -- having -- these 1st and 2nd internal electrodes -- respectively -- either of the side faces -- the drawer electrode pulled out even upwards is formed.

[0016] In such a multilayer capacitor, in order to solve the technical technical problem mentioned above, it consists of this invention as follows. Namely, at least as for one side of the 1st and 2nd internal electrodes, the external terminal electrode of the side face in which formed at least three drawer electrodes of at least three side faces pulled out even upwards, respectively, and the drawer electrode was pulled out electrically connected to a drawer electrode upwards is respectively prepared among four side faces as an above-mentioned drawer electrode.

[0017] In this invention, the 1st above-mentioned internal electrode forms preferably 1st at least three drawer electrode of at least three side faces pulled out even upwards, respectively respectively among four side faces as a drawer electrode. And the 1st external terminal electrode of at least three side faces in which the drawer electrode of these 1st was pulled out electrically connected to the 1st drawer electrode as an external terminal electrode upwards is prepared, respectively. Moreover, the 2nd internal electrode also forms respectively 2nd at least three drawer electrode of at least three side faces pulled out even upwards, respectively among four side faces as a drawer electrode. And the 2nd external terminal electrode electrically connected to the 2nd drawer electrode is prepared in a different location from the location in which at least three side faces in which the drawer electrode of these 2nd was pulled out are

tops respectively, and the 1st external terminal electrode was prepared, respectively.
[0018] in this invention, more preferably, the 1st internal electrode forms 1st at least four drawer electrode pulled out even on four each of a side face, respectively, and the 1st external terminal electrode is prepared in connection with it on each of four side faces where the 1st drawer electrode was pulled out. Similarly, the 2nd external terminal electrode has respectively the more desirable thing of four side faces in which formed 2nd at least four drawer electrode of four side faces pulled out even upwards, respectively, and the 2nd drawer electrode was pulled out in connection with it established upwards respectively also about the 2nd internal electrode.
[0019] Moreover, preferably, all the 1st external terminal electrode is arranged so that the 2nd external terminal electrode may be adjoined on each side face in which the 1st external terminal electrode concerned was prepared. Moreover, all the 1st external terminal electrode and all the 2nd external terminal electrode are more preferably arranged by turns through four side faces.
[0020] Moreover, the number of the parts of the 1st internal electrode and the 2nd internal electrode which counter may be made into plurality so that two or more capacitor units in which parallel connection was carried out by at least one side of the 1st and 2nd external terminal electrodes may be formed. Moreover, one [ at least ] drawer electrode of the 1st and 2nd internal electrodes may be pulled out by at least two on at least one side face.
[0021] Moreover, the multilayer capacitor concerning this invention may be further equipped with the 3rd internal electrode which counters through a specific dielectric layer at least to one side of the 1st and 2nd internal electrodes. In this case, 3rd at least two drawer electrode of at least two side faces pulled out even upwards, respectively is formed, and, as for the 3rd internal electrode, the 3rd external terminal electrode of the side face in which the 3rd drawer electrode was pulled out electrically connected to the 3rd drawer electrode upwards is prepared respectively.
[0022] In the operation gestalt mentioned above, all the 1st external terminal electrode, all the 2nd external terminal electrode, and all the 3rd external terminal electrode are arranged preferably, repeating the same array sequence through four side faces. In this invention, if it sees from another aspect of affairs, as for all external terminal electrodes, it is desirable to be arranged so that the external terminal electrode which makes common the internal electrode connected to this may not be adjoined.
[0023] Moreover, in this invention, if it sees from another aspect of affairs, it is desirable that an external terminal electrode is prepared [ of four side faces ] upwards, respectively.
[0024]
[Embodiment of the Invention] Drawing 1 thru/or drawing 3 show the multilayer capacitor 31 by the 1st operation gestalt of this invention. Considerable [ of drawing 1 thru/or drawing 3 ] is carried out to drawing 15 thru/or drawing 17 mentioned above here, respectively, drawing 1 is the top view showing the appearance of a multilayer capacitor 31, drawing 2 is the top view in which having the 1st cross section and showing the internal structure of a multilayer capacitor 31, and drawing 3 is the top view showing the internal structure of a multilayer capacitor 31 with the 2nd cross section where the 1st cross sections differ.
[0025] The multilayer capacitor 31 is equipped with the body 38 of a capacitor of the shape of a rectangular parallelepiped which has four side faces 34, 35, 36, and 37 which connect between two principal planes 32 and 33 which carry out phase opposite, these principal planes 32, and 33 like the multilayer capacitor 1 mentioned above as the appearance is shown in drawing 1 . The body 38 of a capacitor was prolonged in the direction of principal planes 32 and 33, for example, is equipped with two or more dielectric layers 39 which consist of a ceramic dielectric, and at least one pair of 1st and 2nd internal electrodes 40 and 41 which counter mutually through the specific dielectric layer 39 so that a capacitor unit may be formed.
[0026] Drawing 2 shows the cross section along which the 1st internal electrode 40 passes, and drawing 3 shows the cross section along which the 2nd internal electrode 41 passes. The 1st internal electrode 40 forms respectively the 1st six drawer electrode 42, 43, 44, 45, 46, and 47 of four side faces 34-37 pulled out even upwards, respectively. More, the drawer electrodes 42 and 43 are pulled out even on a side face 34, the drawer electrode 44 is pulled out even on a side face 35, the drawer electrodes 45 and 46 are pulled out by the detail even on a side face 36, and the drawer electrode 47 is pulled out even on the side face 37.
[0027] Moreover, the 1st external terminal electrode 48, 49, 50, 51, 52, and 53 of the side faces 34-37 in which the 1st above-mentioned drawer electrode 42-47 was pulled out electrically connected to the drawer electrodes 42-47 of these 1st upwards is formed, respectively. That is, the external terminal electrodes 48 and 49 are connected to the drawer electrodes 42 and 43 on a side face 34, respectively, the

external terminal electrode 50 is connected to the drawer electrode 44 on a side face 35, the external terminal electrodes 51 and 52 are connected to the drawer electrodes 45 and 46 on a side face 36, respectively, and the external terminal electrode 53 is connected to the drawer electrode 47 on the side face 37.

[0028] On the other hand, the 2nd internal electrode 41 forms respectively the 2nd six drawer electrode 54, 55, 56, 57, 58, and 59 of four side faces 34-37 pulled out even upwards, respectively. More, the drawer electrodes 54 and 55 are pulled out even on a side face 34, the drawer electrode 56 is pulled out even on a side face 35, the drawer electrodes 57 and 58 are pulled out by the detail even on a side face 36, and the drawer electrode 59 is pulled out even on the side face 37.

[0029] Each location on the side face 34-37 in which the 2nd drawer electrode 54-59 mentioned above is pulled out, respectively is carried out if each location where the 1st drawer electrode 42-47 is pulled out, respectively is **. Moreover, the 2nd external terminal electrode 60, 61, 62, 63, 64, and 65 of the side faces 34-37 in which the 2nd above-mentioned drawer electrode 54-59 was pulled out electrically connected to the drawer electrodes 54-59 of these 2nd upwards is respectively formed in a location which is different in the 1st external terminal electrode 48-53. The external terminal electrodes 60 and 61 are connected to the drawer electrodes 54 and 55 on a side face 34, respectively, the external terminal electrode 62 is connected to the drawer electrode 56 on a side face 35, the external terminal electrodes 63 and 64 are connected to the drawer electrodes 57 and 58 on a side face 36, respectively, and the external terminal electrode 65 is connected to the drawer electrode 59 on the side face 37.

[0030] thus, it is arranged so that all the 1st external terminal electrode 48-53 may adjoin the 2nd external terminal electrode 60-65 on four each of side faces 34-37. Moreover, if it sees from another viewpoint, it is arranged so that what carries out all the external terminal electrodes 48-53 and the internal electrode of 60-65 connected for the ability of each coming in common may not be adjoined. If it is on the side face 34 in which the 1st two drawer electrode 42 and 43 and the 2nd two drawer electrode 54 and 55 were pulled out especially The 1st external terminal electrode 48 and 49 and the 2nd external terminal electrode 60 and 61 are arranged by turns. Moreover, if it is on the side face 36 in which the 1st two drawer electrode 45 and 46 and the 2nd two drawer electrode 57 and 58 were pulled out, the 1st external terminal electrode 51 and 52 and the 2nd external terminal electrode 63 and 64 are arranged by turns. Furthermore, also when it sees through four side faces 34-37, the 1st external terminal electrode 48-52 and the 2nd external terminal electrode 60-65 are arranged by turns.

[0031] In order to obtain a bigger capacity, the number of the parts of the 1st internal electrode 40 and the 2nd internal electrode 41 which counter is made into plurality, and it is made to have two or more capacitor units formed in such a multilayer capacitor 31. namely, the time of one either of the 1st and 2nd internal electrodes 40 and 41 being formed in the body 38 of a capacitor -- either of the 1st and 2nd internal electrodes 40 and 41 -- when two tend to be formed or you are going to obtain a still larger capacity so that another side may sandwich this, let the number of the groups of the 1st and 2nd internal electrodes 40 and 41 be plurality. Thus, when the number of the parts of the 1st internal electrode 40 and the 2nd internal electrode 41 which counter is made into plurality, parallel connection of two or more capacitor units is carried out by either [ at least ] the 1st external terminal electrode 48-53 or the 2nd external terminal electrode 60-65.

[0032] In addition, the external terminal electrodes 48-53, and 60-65 are formed, respectively so that it may extend even in the one section each of not only a side-face 34-37 top but both the principal planes 32 and 33. Drawing 4 is drawing corresponding to drawing 18 mentioned above, and shows in illustration the current which flows in this multilayer capacitor 31 with the top view equivalent to drawing 3 . In drawing 4 , the 1st internal electrode 40 is shown by the broken line, and the 2nd internal electrode 41 is shown by the continuous line, and after these have piled up, it is illustrated.

[0033] In drawing 4 , with the arrow head, as the typical path and typical direction are shown, the current shall flow toward each of the 1st external terminal electrode 48-53 from each of the 2nd external terminal electrode 60-65 at the illustrated condition or the time. Thus, when a current flows, induction of the magnetic flux it is decided in the direction of a current that the direction will be is carried out as everyone knows, therefore a self-inductance component arises.

[0034] In the center section 66 of the internal electrodes 40 and 41 shown by O with reference to drawing 4 , since a current flows in the various directions and the magnetic flux in which induction is carried out by the current is offset, there is almost no generating of magnetic flux. This is substantially [ as the case of the former shown in drawing 18 ] the same. Moreover, although a current is in the inclination which separates from each of the 2nd external terminal electrode 60-65 toward each of the 1st external terminal electrode 48-53 the external terminal electrodes 48-53 and near 60-65, the current which flows leftward

by drawing 4 with the breadth of 180 abbreviation, and the current which flows rightward exist. Therefore, the most is offset, consequently magnetic flux does not bring about generating of serious magnetic flux. The same is substantially [ as the case of the former shown in drawing 18 ] said of this.
[0035] In drawing 4 , the big difference with the conventional case shown in drawing 18 is in each edge 67 of right and left [ / near each / of side faces 35 and 37 / (i.e., drawing 4 ) ]. In these edges 67, since the 1st external terminal electrode 50 and 53 and the 2nd external terminal electrode 62 and 65 are formed, there is no flow of the conspicuous current and, similarly near each [ of other side faces 34 and 35 ] generating of serious magnetic flux is not brought about.
[0036] Therefore, according to the multilayer capacitor 31 shown in drawing 1 thru/or drawing 3 , magnetic flux is offset over the whole surface from the center section 66 of the internal electrodes 40 and 41 to an edge 67, and ESL can be stopped very low. Moreover, each of the 1st drawer electrode 42-47 or the 1st external terminal electrode 48-53, With each of the 2nd drawer electrode 54-59 with which a polarity differs from these, or the 2nd external terminal electrode 60-64 Since it can arrange to near mutually and mutual distance can be shortened, current length can be shortened and the self-inductance component generated among these also by this can be made low.
[0037] Drawing 5 thru/or drawing 7 show the multilayer capacitor 71 by the 2nd operation gestalt of this invention. Drawing 5 is the top view showing the appearance of a multilayer capacitor 71 here, drawing 6 is the top view in which having the 1st cross section and showing the internal structure of a multilayer capacitor 71, and drawing 7 is the top view showing the internal structure of a multilayer capacitor 71 with the 2nd cross section where the 1st cross sections differ.
[0038] Considerable [ of drawing 5 thru/or drawing 7 ] is carried out to drawing 1 thru/or drawing 3 which shows the 1st operation gestalt, respectively, in drawing 5 thru/or drawing 7 , the same reference mark is given to the element equivalent to the element shown in drawing 1 thru/or drawing 3 , and the overlapping explanation is omitted. In the multilayer capacitor 71 by this 2nd operation gestalt, 1st internal electrode 40a forms respectively the 1st five drawer electrode 42, 43, 45, 46, and 47a of three side faces 34, 36, and 37 pulled out even upwards, respectively. If difference with the multilayer capacitor 31 by the 1st operation gestalt is said, with this multilayer capacitor 71, there is no drawer electrode equivalent to the drawer electrode 44 pulled out even on a side face 35, drawer electrode 47a pulled out by even the side face 37 is pulled out by the center section of the side face 37, and the drawer electrode 47 is carried out, if that location is **.
[0039] Moreover, the 1st five external terminal electrode 48, 49, 51, 52, and 53a of three side faces 34, 36, and 37 in which the 1st above-mentioned drawer electrode 42-47a was pulled out electrically connected to these 1st five drawer electrodes 42-47a upwards is formed, respectively. If difference with the multilayer capacitor 31 by the 1st operation gestalt is said, with this multilayer capacitor 71, there is no external terminal electrode equivalent to the 1st external terminal electrode 50, and if that location is **, as for external terminal electrode 53a, it is carried out, as for the external terminal electrode 53.
[0040] On the other hand, 2nd internal electrode 41a forms respectively the 2nd five drawer electrode 54, 55, 56a, 57, and 58 of three side faces 34-36 pulled out even upwards, respectively. If difference with the multilayer capacitor 31 by the 1st operation gestalt is said, with this multilayer capacitor 71, there is no drawer electrode equivalent to the drawer electrode 59 pulled out even on a side face 37, drawer electrode 56a pulled out by even the side face 35 is pulled out by the center section of the side face 37, and the drawer electrode 56 is carried out, if that location is **.
[0041] Moreover, the 2nd external terminal electrode 60, 61, 62a, 63, and 64 of three side faces 34-36 in which the 2nd above-mentioned drawer electrode 54-58 was pulled out electrically connected to the drawer electrodes 54-58 of these 2nd upwards is formed, respectively. If difference with the multilayer capacitor 31 by the 1st operation gestalt is said, with this multilayer capacitor 71, there is no external terminal electrode equivalent to the 2nd external terminal electrode 65, and if that location is **, as for external terminal electrode 62a, it is carried out, as for the external terminal electrode 62.
[0042] In order to obtain a bigger capacity, the number of the parts of 1st internal electrode 40a and 2nd internal electrode 41a which counter is made into plurality, and it is made to have two or more capacitor units formed also in such a multilayer capacitor 71. And parallel connection of the capacitor unit of these plurality is carried out by either [ at least ] the 1st external terminal electrode 48-53a or the 2nd external terminal electrode 60-64.
[0043] according to this 2nd operation gestalt, it is arranged so that each of the 1st external terminal electrode 48, 49, 51, and 52 may adjoin either of the 2nd external terminal electrode 60, 61, 63, and 64 on two each of side faces 34 and 36. Moreover, although only 2nd external terminal electrode 62a is located on a side face 35 and only 1st external terminal electrode 53a is only located on a side face 37 Thus, by

locating the external terminal electrodes 62a and 53a also in side faces 35 and 37, respectively If compared with the conventional multilayer capacitor 1 shown in drawing 15 thru/or drawing 17 at least, while being able to turn the flow of the current on internal electrode 40a and 41a in the more various directions and being able to offset more magnetic flux Since current length can be shortened more, an inductance component can be reduced more.

[0044] Drawing 8 thru/or drawing 11 show the multilayer capacitor 81 by the 3rd operation gestalt of this invention. Drawing 8 is the top view showing the appearance of a multilayer capacitor 81 here, drawing 9 is the top view in which having the 1st cross section and showing the internal structure of a multilayer capacitor 81, drawing 10 is the top view showing the internal structure of a multilayer capacitor 81 with the 2nd cross section where the 1st cross sections differ, and drawing 11 is the top view showing the internal structure of a multilayer capacitor 81 with the 3rd cross section where the 1st and 2nd cross sections differ.

[0045] In drawing 8 thru/or drawing 11 , the same reference mark is given to the element equivalent to the element shown in drawing 1 thru/or drawing 3 , and the overlapping explanation is omitted. The multilayer capacitor 81 by this 3rd operation gestalt is characterized by having further the 3rd internal electrode 82 which counters through the specific dielectric layer 39 at least to one side of the 1st and 2nd internal electrodes 40b and 41b. This 3rd internal electrode 82 forms respectively the 3rd four drawer electrode 83, 84, 85, and 86 of two side faces 34 and 36 pulled out even upwards, respectively. More, the drawer electrodes 83 and 84 are pulled out even on a side face 34, and the drawer electrodes 85 and 86 are pulled out by the detail even on the side face 36.

[0046] Moreover, the 3rd external terminal electrode 87, 88, 89, and 90 of the side faces 34 and 36 in which the 3rd above-mentioned drawer electrode 83-86 was pulled out electrically connected to the drawer electrodes 83-86 of these 1st upwards is formed, respectively. That is, the external terminal electrodes 87 and 88 are connected to the drawer electrodes 83 and 84 on a side face 34, respectively, and the external terminal electrodes 89 and 90 are connected to the drawer electrodes 85 and 86 on the side face 36, respectively. If difference with the multilayer capacitor 31 by the 1st operation gestalt is said, in this multilayer capacitor 81, the 3rd external terminal electrode 88 and 89 is formed in each location in which the 3rd external terminal electrode 87 and 90 was formed in each location in which the 1st external terminal electrode 48 and 52 in a multilayer capacitor 31 was formed, respectively, and the 2nd external terminal electrode 61 and 63 in a multilayer capacitor 31 was formed, respectively.

[0047] On the other hand, about the 1st internal electrode 40b, the 1st four drawer electrode 42b, 44, 45b, and 47 of four side faces 34-37 pulled out even upwards, respectively is formed respectively. If difference with the multilayer capacitor 31 by the 1st operation gestalt is said, as a drawer electrode pulled out even on a side face 34 and 36 in this multilayer capacitor 81, there will be only every one drawer electrodes 42b and 45b, respectively.

[0048] Moreover, the 1st four external terminal electrode 48b, 50, 51b, and 53 of four side faces 34-37 in which the 1st above-mentioned drawer electrode 42b-47 was pulled out electrically connected to these 1st four drawer electrodes 42b-47 upwards is formed, respectively. If difference with the multilayer capacitor 31 by the 1st operation gestalt is said, in this multilayer capacitor 81, the 1st external terminal electrode 48b and 51b is formed in each location in which the 2nd external terminal electrode 60 and 64 in a multilayer capacitor 31 was formed, respectively.

[0049] Moreover, about the 2nd internal electrode 41b, the 2nd four drawer electrode 54b, 56, 57b, and 59 of four side faces 34-37 pulled out even upwards, respectively is formed respectively. If difference with the multilayer capacitor 31 by the 1st operation gestalt is said, as a drawer electrode pulled out even on a side face 34 and 36 in this multilayer capacitor 81, there will be only every one drawer electrodes 54b and 57b, respectively.

[0050] Moreover, the 2nd four external terminal electrode 60b, 62, 63b, and 65 of four side faces 34-37 in which the 2nd above-mentioned drawer electrode 54b-59 was pulled out electrically connected to these 1st four drawer electrodes 54b-59 upwards is formed, respectively. If difference with the multilayer capacitor 31 by the 1st operation gestalt is said, in this multilayer capacitor 81, the 2nd external terminal electrode 60b and 63b is formed in each location in which the 1st external terminal electrode 49 and 51 in a multilayer capacitor 31 was formed, respectively.

[0051] In this multilayer capacitor 81, a laminating is carried out to the order of the 3rd internal electrode 82, the 1st internal electrode the 40b, and 2nd internal electrode 41b. It lets four side faces 34-37 pass, and the same array sequence of either of the 3rd external terminal electrode 87-90, either of the 1st external terminal electrode 48b-53, and either of the 2nd external terminal electrode 60b-65 is repeated by this. In addition, above-mentioned built-up sequence can be changed into arbitration.

[0052] Moreover, also in a multilayer capacitor 81, in order to obtain a bigger capacity, let the number of the capacitor units formed of each opposite of the 3rd internal electrode 82, the 1st internal electrode the 40b, and 2nd internal electrode 41b be plurality. Therefore, repeat only the 3rd internal electrode 82 and internal electrode 40of ** 1st b two or more times, and they carry out a laminating, or Repeat only the 1st internal electrode 40b and 2nd internal electrode 41b two or more times, and they carry out a laminating, or Only the 2nd internal electrode 41b and the 3rd internal electrode 82 can be repeated two or more times, and can carry out a laminating, or the 3rd internal electrode 82, 1st internal electrode 40b, and 2nd internal electrode 41b can be repeated two or more times, and can carry out a laminating. And even if there are few 3rd external terminal electrodes 87-90, 1st external terminal electrodes 48b-53, and 2nd external terminal electrodes 60b-65, parallel connection of the capacitor unit of these plurality is carried out by either.

[0053] also in this 3rd operation gestalt, like the 1st operation gestalt, it connects with a mutually different internal electrode, namely, the external terminal electrode which has a mutually different polarity is located on four each of side faces 34-37. 1st external terminal electrode 48b, 2nd external terminal electrode 60b, and the 3rd external terminal electrode 87 and 88 are located more on a side face 34 at a detail, and it sets on a side face 35. The 1st external terminal electrode 50 and the 2nd external terminal electrode 62 are located, and it sets on a side face 36. 1st external terminal electrode 51b, 2nd external terminal electrode 63b, and the 3rd external terminal electrode 89 and 90 are located, and the 1st external terminal electrode 53 and the 2nd external terminal electrode 65 are located on a side face 37.

[0054] Therefore, since current length can be shortened while being able to offset magnetic flux effectively also according to this 3rd operation gestalt by turning the flow of the current on internal electrode 40b and 41b in the various directions, reduction of an inductance component can be aimed at. in addition, unlike the 1st operation gestalt, with this 3rd operation gestalt, a different polar external terminal electrode in all parts adjoins each other mutually -- as, although not arranged If compared with the conventional multilayer capacitor 1 shown in drawing 15 thru/or drawing 17 at least, since the flow of the current on an internal electrode 40 and 41 can be turned in the more various directions and current length can be shortened more, an inductance component can be reduced more.

[0055] Moreover, as a modification of the 3rd operation gestalt, it cannot have the 3rd internal electrode 82, but can also consider as the multilayer capacitor which carried out the laminating only of the 1st and 2nd internal electrodes 40b and 41b. Furthermore, the drawer electrode further pulled out by the 3rd internal electrode 82 on side faces 35 and 37 may be formed. Drawing 12 thru/or drawing 14 show the multilayer capacitor 91 by the 4th operation gestalt of this invention. Drawing 12 is the top view showing the appearance of a multilayer capacitor 91 here, drawing 13 is the top view in which having the 1st cross section and showing the internal structure of a multilayer capacitor 91, and drawing 14 is the top view showing the internal structure of a multilayer capacitor 91 with the 2nd cross section where the 1st cross sections differ.

[0056] Considerable [ of drawing 12 thru/or drawing 14 ] is carried out to drawing 1 thru/or drawing 3 which shows the 1st operation gestalt, respectively, in drawing 12 thru/or drawing 14 , the same reference mark is given to the element equivalent to the element shown in drawing 1 thru/or drawing 3 , and the overlapping explanation is omitted. The multilayer capacitor 91 by this 4th operation gestalt is similar in appearance with the multilayer capacitor 71 by the 2nd operation gestalt. 1st internal electrode 40c forms respectively the 1st five drawer electrode 42, 43, 44c, 45c, and 46c of three side faces 34, 35, and 36 pulled out even upwards, respectively. If difference with the multilayer capacitor 31 by the 1st operation gestalt is said, with this multilayer capacitor 91, there is no drawer electrode equivalent to the drawer electrode 47 pulled out even on a side face 37, and if each of that location is **, as for the drawer electrodes 44c, 45c, and 46c pulled out by even side faces 35 and 36, respectively, it is carried out, as for the drawer electrodes 44-46.

[0057] Moreover, the 1st five external terminal electrode 48, 49, 50c, 51c, and 52c of three side faces 34-36 in which the 1st above-mentioned drawer electrode 42-46c was pulled out electrically connected to these 1st five drawer electrodes 42-46c upwards is formed, respectively. If difference with the multilayer capacitor 31 by the 1st operation gestalt is said, with this multilayer capacitor 91, there is no external terminal electrode equivalent to the 1st external terminal electrode 53, and if each of that location is **, as for the external terminal electrodes 50c, 51c, and 52c, it is carried out, as for the external terminal electrodes 50-52.

[0058] On the other hand, 2nd internal electrode 41c forms respectively the 2nd five drawer electrode 54, 55, 57c, 58c, and 59c of three side faces 34, 36, and 37 pulled out even upwards, respectively. If difference with the multilayer capacitor 31 by the 1st operation gestalt is said, with this multilayer

capacitor 91, there is no drawer electrode equivalent to the drawer electrode 59 pulled out even on a side face 35, and if each of that location is **, as for the drawer electrodes 57c, 58c, and 59c pulled out by even side faces 34, 36, and 37, it is carried out, as for the drawer electrodes 57-59.
[0059] Moreover, the 2nd external terminal electrode 60, 61, 63c, 64c, and 65c of three side faces 34, 36, and 37 in which the 2nd above-mentioned drawer electrode 54-59c was pulled out electrically connected to the drawer electrodes 54-59c of these 2nd upwards is formed, respectively. If difference with the multilayer capacitor 31 by the 1st operation gestalt is said, with this multilayer capacitor 91, there is no external terminal electrode equivalent to the 2nd external terminal electrode 62, and if each of that location is **, as for the external terminal electrodes 63c, 64c, and 65c, it is carried out, as for the external terminal electrodes 63-65.
[0060] In order to obtain a bigger capacity, the number of the parts of 1st internal electrode 40c and 2nd internal electrode 41c which counter is made into plurality, and it is made to have two or more capacitor units formed also in such a multilayer capacitor 91. And parallel connection of the capacitor unit of these plurality is carried out by either [ at least ] the 1st external terminal electrode 48-52c or the 2nd external terminal electrode 60-65c.
[0061] With this 4th operation gestalt, either of the 1st external terminal electrode 48-52c and either of the 2nd external terminal electrode 60-65c are arranged by turns through four side faces 34-37 like the 1st operation gestalt mentioned above. In this point, it differs from the 2nd operation gestalt. Therefore, while according to the 4th operation gestalt being able to turn the flow of the current on internal electrode 40c and 41c in the various directions and being able to offset magnetic flux effectively like the 1st operation gestalt, current length can be shortened and an inductance component can be reduced by this.
[0062] Each sample of the multilayer capacitor 31 (example 1) concerning the 1st operation gestalt and the multilayer capacitor 71 (example 2) concerning the 2nd operation gestalt which were explained above, the multilayer capacitor 81 (example 3) concerning the 3rd operation gestalt, the multilayer capacitor 91 (example 4) concerning the 4th operation gestalt, and the conventional multilayer capacitor 1 (example of a comparison) was produced, and each ESL was evaluated.
[0063] What each sample set the appearance flat-surface dimension to 3.2mmx2.5mm, and carried out 6 laminatings of the internal electrode in total here, Namely, if it is in some which have two kinds of internal electrodes like multilayer capacitors 31, 71, 91, and 1 (examples 1, 2, and 4 and example of a comparison) The laminating of two kinds of internal electrodes was repeated 3 times, and if it was in some which have three kinds of internal electrodes like a multilayer capacitor 81 (example 3), the laminating of three kinds of internal electrodes should be repeated twice.
[0064] Moreover, ESL was calculated with the resonance method. the multilayer capacitor which serves as a resonance method with each sample -- the frequency characteristics of an impedance -- measuring -- frequency f0 of the minimum point (it is called the series resonance point between the capacity components CS and ESL of a capacitor.) from -- ESL= -- 1/[(2pif0) 2 xCS]
It is the approach of calculating ESL as being alike.
[0065] The ESL measured value of each sample is shown in the following table 1.
[0066]
[Table 1]

| | ESL値 (pH) |
|---|---|
| 実施例1 | 40 |
| 実施例2 | 72 |
| 実施例3 | 85 |
| 実施例4 | 51 |
| 比較例 | 95 |

As for examples 1-4, in Table 1, the effectiveness which ESL was low stopped by each compared with the example of a comparison, and was most excellent about reduction of ESL especially shows that the example 1 is shown. Moreover, if an example 4 is compared with an example 1, although it is inferior, it shows the more excellent effectiveness about reduction of ESL compared with examples 2 and 3.
[0067] as mentioned above, although explained in relation to the operation gestalt illustrating this invention, various the locations and number of external terminal electrodes can be boiled, corresponding

to it in boiling and changing various the locations and number of a drawer electrode of internal electrodes ****, for example, it can change within the limits of this invention.

[0068]

[Effect of the Invention] According to this invention, as mentioned above, at least one side of the 1st and 2nd internal electrodes At least three drawer electrodes of at least three side faces pulled out even upwards, respectively are respectively formed among four side faces of the body of a capacitor. Moreover, since the external terminal electrode of the side face in which such a drawer electrode was pulled out, respectively respectively connected to a drawer electrode electrically upwards is prepared, respectively Since current length can be shortened while being able to offset magnetic flux effectively by turning the flow of the current on an internal electrode in the various directions, ESL can be made small.

[0069] Therefore, resonance frequency can be RF-ized. The multilayer capacitor which means that the frequency region which functions as a capacitor high-frequency-izes this, therefore is applied to this invention can respond to high frequency-ization of an electronic circuitry enough, for example, can be advantageously used as the bypass capacitor in a high frequency circuit, and a decoupling capacitor. Moreover, since the multilayer capacitor concerning this invention is low ESL although the function (function in which power, such as the time of a standup, supplies suddenly quantity of electricity charged by the capacitor by the way to the power which is the need) as a quick power supply is also required if it is in the decoupling capacitor used for MPU (microprocessing unit) etc., when turned to such an application, it can respond to rapidity enough.

[0070] In this invention, each following embodiment raises more offset of magnetic flux which was mentioned above, or shortens current length more, and is effective by reduction of ESL. It is the embodiment in which the external terminal electrode of at least three side faces in which formed at least three drawer electrodes of at least three side faces pulled out even upwards, respectively among four side faces of the body of a capacitor, and these drawers electrode was pulled out about the both sides of the 1st and 2nd internal electrodes by the 1st, respectively respectively connected to a drawer electrode electrically upwards is prepared, respectively.

[0071] the 1st 2nd above-mentioned operative condition -- it is the operation gestalt with which it sets like, the 1st internal electrode forms 1st at least four drawer electrode pulled out even on four each of a side face, respectively, and the 1st external terminal electrode is prepared in connection with it on each of four side faces where the 1st drawer electrode was pulled out. the 1st above-mentioned operative condition same with the 3rd -- it is the embodiment in which it sets like, the 2nd internal electrode forms 2nd at least four drawer electrode pulled out even on four each of a side face, respectively, and the 2nd external terminal electrode is prepared in connection with it on each of four side faces where the 2nd drawer electrode was pulled out.

[0072] In addition, about the both sides of these 1st and 2nd internal electrodes, if the above configurations are adopted, it is much more effective. It is the embodiment by which all the 1st external terminal electrode is arranged the 4th so that the 2nd external terminal electrode may be adjoined on each side face in which the 1st external terminal electrode concerned was prepared. If it lets four side faces pass and all the 1st external terminal electrode and all the 2nd external terminal electrode are arranged by turns at this time, in addition, it is effective.

[0073] It is the embodiment in which one [ at least ] drawer electrode of the 1st and 2nd internal electrodes is pulled out by the 5th at least two on at least one side face. It is the embodiment arranged the 6th so that the external terminal electrode with which all external terminal electrodes make common the internal electrode connected to this may not adjoin each other. An external terminal electrode is the embodiment of four side faces established upwards, respectively the 7th.

[0074] Moreover, in this invention, if the number of the parts of the 1st internal electrode and the 2nd internal electrode which counter is made into plurality so that two or more capacitor units in which parallel connection was carried out by at least one side of the 1st and 2nd external terminal electrodes may be formed, it is effective in a miniaturization and high-capacity-izing of a multilayer capacitor. In this invention, it has further the 3rd internal electrode which counters through a specific dielectric layer at least to one side of the 1st and 2nd internal electrodes. Moreover, the 3rd internal electrode 3rd at least two drawer electrode of at least two side faces pulled out even upwards, respectively is formed respectively. Since current length can be shortened while being able to offset magnetic flux effectively even if the 3rd external terminal electrode of the side face in which the 3rd drawer electrode was pulled out electrically connected to the 3rd drawer electrode upwards is prepared, respectively, the effectiveness which makes ESL small is respectively expectable.

[0075] In the operation gestalt mentioned above, since current length can be shortened more while being

able to offset magnetic flux more effectively if all the 1st external terminal electrode, all the 2nd external terminal electrode, and all the 3rd external terminal electrode are arranged repeating the same array sequence through four side faces, ESL can be made smaller.

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[Translation done.]

* NOTICES *

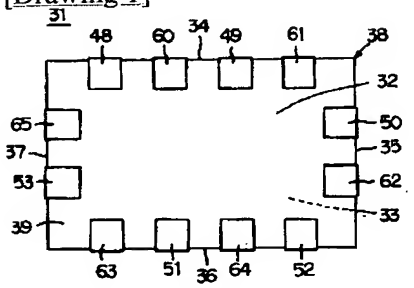


1.This document has been translated by computer. So the translation may not reflect the original precisely.

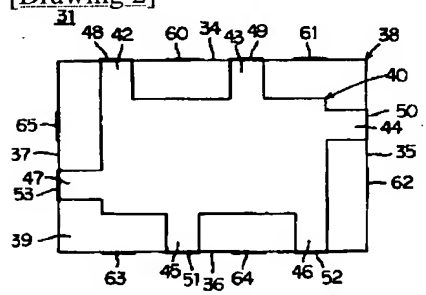
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

## DRAWINGS

[Drawing 1]




[Drawing 2]

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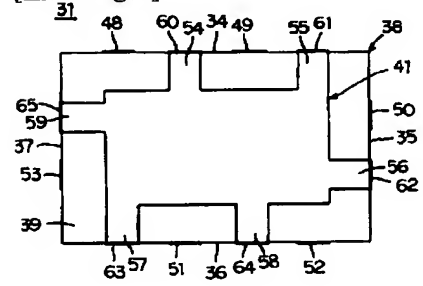


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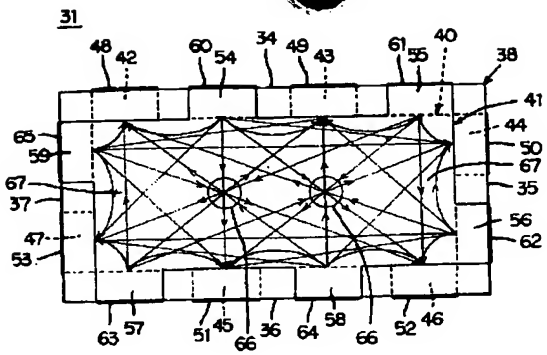
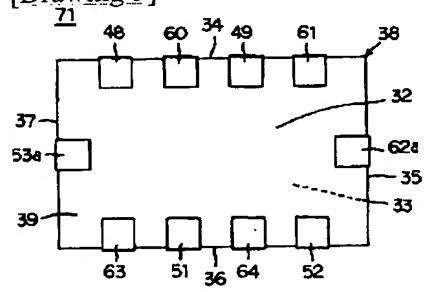



[Drawing 5]

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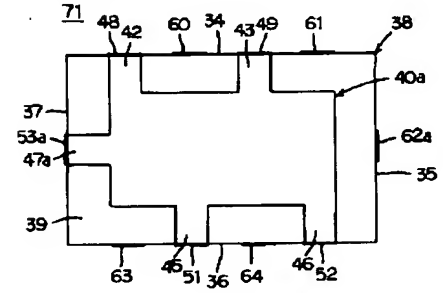


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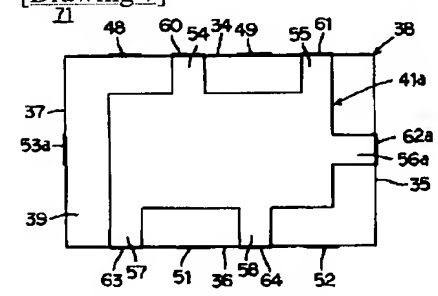
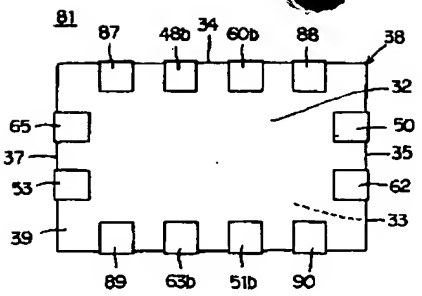



[Drawing 8]

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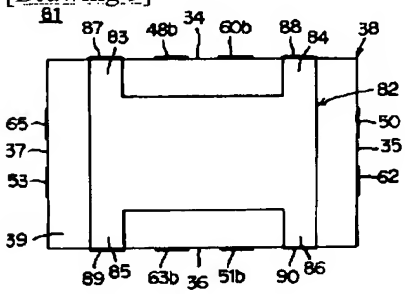
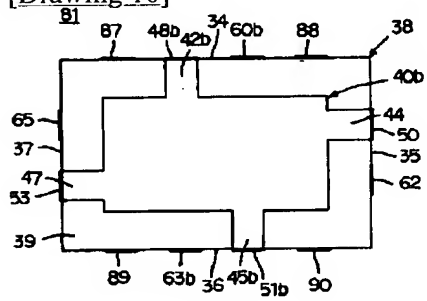



[Drawing 10]

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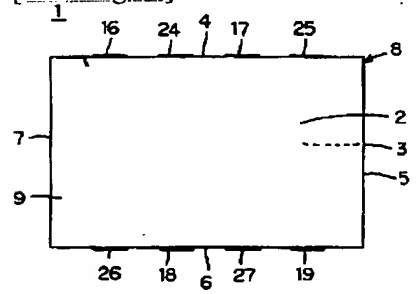


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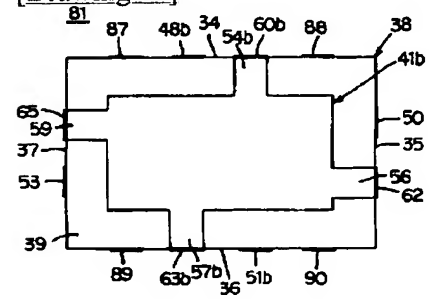
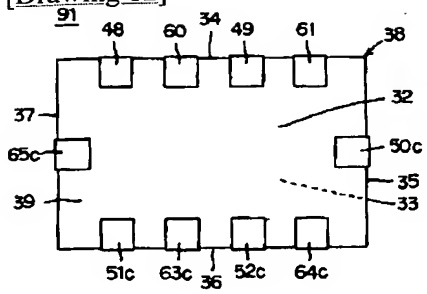
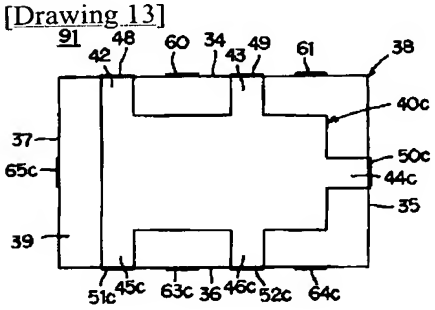


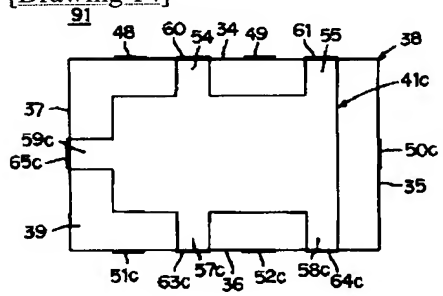
[Drawing 12]



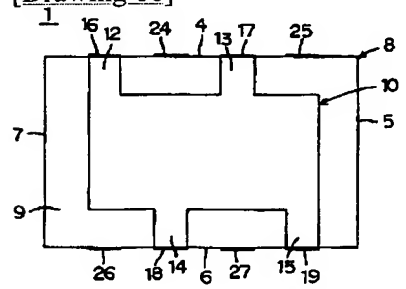

[Drawing 13]



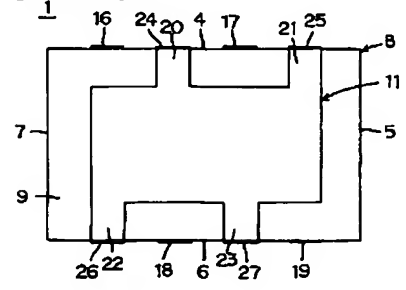

[Drawing 14]



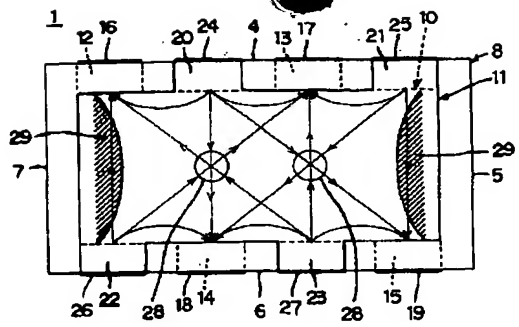

[Drawing 16]




[Drawing 17]




[Drawing 18]




[Translation done.]